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## **EUROPEAN PATENT APPLICATION**

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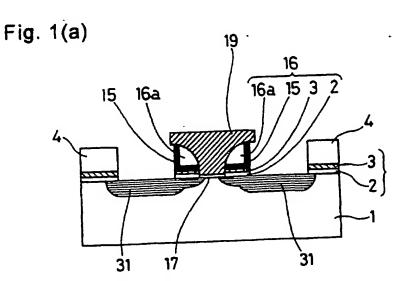
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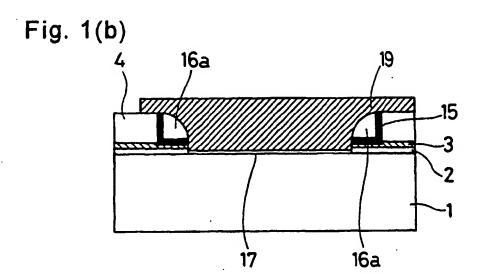
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## (54) MOS transistor and fabrication process therefor

(57) An MOS transistor comprises a semiconductor substrate having a field region; a gate electrode (19) formed on the semiconductor substrate (1) through the intermediatry of a gate insulating film; and source/drain regions (31) formed in the semiconductor substrate; wherein the field region including at least a lower insulating film (3,2) and an upper insulating film (4) made of a material permitting the upper insulating film to be selectively etched with respect to the lower insulating film; the gate electrode being configured such that the gate length of a top surface thereof is greater than the gate

length of a bottom surface thereof facing a channel region positioned between the source/drain regions; the gate electrode having a sidewall spacer (16) formed of a sidewall insulating layer made of the lower insulating film (3,2) and a material (16a,15) permitting the sidewall insulating layer to be selectively etched with respect to the upper insulating film, the sidewall spacer contacting a side wall of the gate electrode for covering an outer periphery of the channel region; and the channel region being substantially leveled with the source/drain regions.







## **EUROPEAN SEARCH REPORT**

Application Number EP 96 30 5957

	DOCUMENTS CONSIDE		CLASSISICATION OF THE			
Category	Citation of document with in of relevant passa	dication, where appropriate, ges	Rele to d	evant aim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)	
Υ .	HIRONORI TSUKAMOTO ET AL: "SUB 0.1 M NMOSFET UTILIZING NARROW TRENCH GATE AND SELECTIVE EXCIMER LASER ANNEALING (SELA)" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 29 August 1993, pages 26-28, XP000409365 * the whole document *			5	H01L29/78 H01L21/336 H01L29/423 H01L21/265 H01L27/092 H01L21/8238 H01L21/762	
Y	PATENT ABSTRACTS OF vol. 012, no. 246 ( -& JP 63 036564 A 17 February 1988 * abstract; figure	E-632), 12 July 1988 (NEC CORP),	1-3,	,5	TECHNICAL FIELDS SEARCHED (Int.Cl.6)	
X	"ADDITIVE PROCESS POLYSILICON GATES" RESEARCH DISCLOSURE no. 305, 1 Septembe XP000070576	, r 1989, page 644	6-8	e		
Α	* the whole documen		1-3	,5		
A	US 5 270 234 A (HSU 14 December 1993 * figures 1-10 *	LOUIS L ET AL)	1,2	,6		
Α	PATENT ABSTRACTS OF vol. 018, no. 545 ( 18 October 1994 -& JP 06 196691 A 15 July 1994 * abstract; figures	E-1617), (SONY CORP),	1-3	,5		
А	PATENT ABSTRACTS OF vol. 013, no. 218 ( -& JP 01 030270 A 1 February 1989 * abstract; figure	E-761), 22 May 1989 (FUJITSU LTD),	6			
	The present search report has	been drawn up for all claims				
		Date of completion of the searc	completion of the search		Examiner	
	THE HAGUE	7 December 199	8	Gé	lébart, J	
X:pa Y:pa dox A:teo O:no	CATEGORY OF CITED DOCUMENTS ricularly relevant if taken alone ricularly relevant if combined with and cument of the same category shotogical background n-written disclosure ermediate document	E : earner parel after the filir ther D : document of L : document of	ni document ig date ited in the a ited for othe	but put pplication reason	biished on, or n	



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		ERED TO BE RELEVANT		OLA COLENATION OF THE
Category	Citation of document with it of relevant pass	ndication, where appropriate, ages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Im.CL6)
<b>A</b> .	DE 44 15 137 C (GOL 20 July 1995 # figure 2 #	D STAR ELECTRONICS)	1,6	
A	US 5 342 803 A (SHI 30 August 1994 * figure 1 *	MOJI NORIYUKI)	1	
A	US 4 942 448 A (TSU AL) 17 July 1990 # figure 12 #	KAMOTO KATSUHIRO ET	1	
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				TECHNICAL FIELDS SEARCHED (Int.CL2)
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	The present search report has	heen drawn un for all claims		
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